Workgroup Server 9150: Memory Bus Operations (4/94)

Revised: 4/26/94
Security: Everyone

Workgroup Server 9150: Memory Bus Operations (4/94)

==========

Article Created: 26 April 1994

TOPIC ----------

This article describes the memory bus operations of the Workgroup Server 9150 (WS 9150).

DISCUSSION ----------

The High speed Memory Controller (HMC) contains a single read/write control register and resets to a "least critical" state to guarantee operation on power up. The HMC supports the basic PowerPC 601 processor's transfer protocol, including all of the PowerPC 601 processor's single beat accesses with the addition of the 4 beat 32 byte cache line access. Only the transfer codes in the basic protocol will generate a response from the HMC. Extended protocol codes will result in a transfer error exception from the WS 9150 I/O controller. The WS 9150 does not support the Little Endian mode of the PowerPC 601 processor.

Misalignment

Misaligned reads from the PowerPC 601 processor are translated into standard double-word reads by the HMC. However misaligned writes are fully decoded so only the appropriate DRAM CAS signals are selected. The L2 cache mirrors this functionality through the cache data RAM asynchronous write-enables so that RAM write hits are updated properly.

Address Only Transaction

The PowerPC 601 processor initiates address-only transactions when instructions that affect the level 1 cache are executed. These transactions never require data bus tenure but do require an address acknowledgment. The HMC decodes the TT(1) input to identify the address only cycles and asserts AACK_ on the third clock following transfer start.

Arbitration

Bus arbitration is fielded by the HMC on the address bus only. Granting of the data bus is implicit based on successful arbitration for the address bus. The PowerPC 601 processor's bus protocol specifies an arbitration overhead of one CPU clock unless bus parking is used. Bus parking is a situation that occurs when bus grant is asserted to a bus master who is not currently requesting the bus. Since the PowerPC 601 processor is the primary WS 9150 bus master, the HMC eliminates one clock of the PowerPC 601 processor's memory latency by parking the PowerPC 601 processor on the bus. The HMC arbitration logic is a simple combinational decode of the bus request signals. Priority of bus granting is fixed in the order of DMA, PDS, and lastly the PowerPC 601 processor. The PowerPC 601 processor is only granted the bus in the absence of other bus requests. As a result the PowerPC 601 processor bus request is not an HMC input. Receiving a bus grant from the HMC does not imply that the bus is unused. It is the responsibility of the requesting device to verify that the bus is indeed free by qualifying bus grant with the de-assertion of ABB_. The WS 9150 adds an extra level of decode in order to have both the VRAM frame buffer and the NuBus controller use the same bus request bus grant lines to HMC. The NuBus controller has priority over the VRAM based frame buffer.

Pipelining

All memory bus transactions are non-pipelined.

Snooping

The primary focus of the WS 9150 is uni-processing, and provisions for snooping would lengthen the latency to 2nd level cached data by 50% (from 2 clocks minimum to 3 clocks). For this reason, snooping of other processor internal caches is not supported on the WS 9150 memory bus. Alternate masters can be designed to snoop the PowerPC 601 processor's internal cache, provided certain restrictions are followed. When the alternate master reads data from DRAM that data must not be forwarded or acted upon until the ARTRY_ window has expired. If the PowerPC 601 processor does assert ARTRY_, then the alternate master discards the read data and backs off the bus allowing the PowerPC 601 processor to update memory. The alternate master then reruns the bus cycle to obtain the updated copy. If the alternate master is writing data to DRAM then an ARTRY_ from the PowerPC 601 processor implies a pipeline collision. The alternate master must retain the data so that the write cycle can continue to be rerun until the PowerPC 601 processor pipeline collision clears. This scenario has the benign side-effect that DRAM is updated with the same data more than once.

Bus Errors

Any access to undecoded address space will result in a Transfer Error Acknowledge (TEA) asserted by FAT AMIC after a 40 µsec time-out. While in 680x0 based Macintosh computer's BERR time-outs where frequently generated by the Slot Manager, SCSI driver, and so on, and were generally recoverable, this is not the case in WS 9150. A cycle terminated with TEA is not in general recoverable due to the more or less independent operation of the Bus Interface, Branch, and Integer Execution Units within the PowerPC 601 processor. To prevent this, the Memory Management Unit (MMU) should be used to map only that space which is decoded by hardware. This can be determined at start-up by testing the various

optional address spaces in the PDS range, using carefully written code. With the proper MMU setup, accesses to undecoded address space will generate an addressing exception from the MMU, which is recoverable. The only changes made to the PDM bus operation for WS 9150 are the expansion of the arbitration to allow for both the NuBus controller and the VRAM based frame buffer. PDM only accommodates one at a time.

Support Information Services

Tech Info Library Article Number:15217