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Token Ring NB/c Card: IBM Chipset Shared Memory Register (4/94)

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TOPIC -----

This article describes the IBM chipset shared memory register on the Apple Token Ring NB/c Card.

DISCUSSION -----

The definitions and addresses of the Shared Memory Control Registers on the IBM module are shown below. Each register is 16 bits, with the upper byte being addressed by an even address (for example 81E00) and the lower byte being addressed by an odd address (for example 81E01). Either byte or word accesses may be used. Refer to section 6.6 of the "Token-Ring Mini-Card Technical Reference" for explanations of these registers. Chapter 7 of the "IBM Local Area Network Technical Reference" has additional information, though the Mini-Card specification supersedes it in the event of a discrepancy. Also note that the bit ordering is different between these two manuals; The former labels the most significant bit as bit "15", while the latter calls the same bit "0".

Address Function

| | |
|-------|---|
| 81E00 | RRR - Shared RAM Relocation Register (set upper byte to "10") |
| 81E02 | WRBR - Write Region Base Address Register |
| 81E04 | WWOR - Write Window Open Register |
| 81E06 | WWCR - Write Window Close Register |
| 81E08 | UISR (ISRP) - User Interrupt Status Register (adapter-to-host) |
| 81E0A | LISR (ISRA) - Adapter Interrupt Status Register (host-to-adapter) |
| 81E0C | TCR - Timer Control Register |
| 81E0E | TVR - Timer Value Register |
| 81E10 | UER - Reserved |
| 81E12 | SRR - Soft Reset Register |
| 81E14 | IVR - Interrupt Vector Register (not used) |
| 81E16 | JR - Jumper Register |
| 81E18 | SRPR - Shared RAM Page Register (set upper byte to "C0") |

The above registers are duplicated 3 times, for a total of 4 banks of registers.

The registers present in each bank are identical, however the operation performed changes based on the bank addressed. The following shows the address ranges of each bank, and the resulting operation.

| Range | Operation |
|-------------|---------------------------|
| ----- | ----- |
| 81E00-81E1F | Read or Write |
| 81E20-81E3F | Read/Reset under mask (0) |
| 81E40-81E5F | Read/Set under mask (1) |
| 81E60-81E7F | Read only |

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